ABSTRACT OF THE DISCLOSURE

A clock extracting part has a first phase comparator circuit, a first up/down counter, a weighting circuit, a charge pump and a low-pass filter forming a voltage value determining part, and a voltage controlled oscillator circuit. A retiming clock generating part has a second up/down counter and a phase switching circuit. Furthermore, a phase adjusting part has a first counter, a second counter, a second phase comparator circuit and a third up/down counter forming a phase adjusting part. A clock data recovery circuit is formed by said clock extracting part, the retiming clock generating part, the phase adjusting part, and a first-in first-out memory part. Thereby, a clock data recovery circuit is obtained, in which jitter transfer characteristics and jitter tolerance satisfy the standards of both the SONET and SDH.